IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of performing a context switch operation, comprising:

accessing context data in a first register of a peripheral system when a context index is set to a first index value;

receiving, by the peripheral system, a second index value from a host computer associated with the peripheral system;

setting the context index to the second index value to perform a context switch;

accessing context data in a second register of the peripheral system when the context index is set to the second index value, wherein the first and second registers are collocated with the peripheral system.

2. (Original) The method recited in claim 1, wherein context data further includes:

a device address for one of a plurality of network devices;

a class value;

a clock offset value; and

an active member address.

3. (Previously Presented) The method recited in claim 1, wherein the accessing context data in a second register further comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripherals system, a control input that identifies at least one of a plurality of functions, the plurality of functions including a read function and a write function;

receiving, by the peripheral system if the control input identifies the write function, a data value; and

if the control input identifies the write function, writing the data value to the second register at the address identified by the address value.

4. (Previously Presented) The method recited in claim 1, wherein the accessing context data in a second register further comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a read control input; and

providing the contexts of the second register at the address identified by the address value to the host computer.

5. (Previously Presented) The method recited in claim 1, wherein the accessing context data in a second register further comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a data value;

receiving, by the peripheral system, a write control input; and

writing the data value to the second register at the address identified by the address value.

6. (Previously Presented) The method recited in claim 1, wherein the accessing context data further comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a control input that identifies one of a plurality of functions, the plurality of functions including a read function and a write function; and

if the control input identifies the read function, providing the contents of the second register at the address identified by the address value to the host computer.

7. (Original) The method recited in claim 1, wherein the first and second registers are not architected registers.

8. (Currently Amended) A system, comprising:

a host computer, the host computer including a microprocessor;

at least one peripheral system coupled to the host processor, the peripheral system including a first register, the first register being associated with a first index value, the peripheral system further including a second register, the second register being associated with a second index value, wherein the first and second registers are collocated with the peripheral system;

an interface coupled to the host computer and to the peripheral system, the interface being configured to provide the first and second index values from the host computer to the peripheral system; and

a register access circuit coupled to the host computer, the register access circuit being configured to access the first register if the first index value is provided by the host computer, the register access circuit being further configured to access the second register if the second index value is provided by the host computer.

9. (Previously Presented) The system recited in claim 8, wherein the first and second register are not architected registers.

10. (Original) The system recited in claim 8, wherein the peripheral system includes a state machine module, the state machine module including:

an address portion;

a control portion; and

a data portion, the first register and the second register being included in the data portion.

11. (Original) The system recited in claim 8, wherein the peripheral system includes a microprocessor.

12. (Previously Presented) The system recited in claim 10, wherein the address portion comprises the register access circuit.

13. (Previously Presented) The system recited in claim 8, wherein the peripheral system includes a plurality of context registers, wherein each of the plurality of context registers is associated with one of a plurality of index values other than the first and second index values.

14. (Previously Presented) The system recited in claim 8, wherein the peripheral system includes at least one index register for storing the first and second index values.

Please add new claims 15-20 as follows.

15. (New) A wireless peripheral system for performing a context switch operation comprising:

a host controller, the host controller further comprising a state machine, wherein the state machine comprises:

a data portion, the data portion including at least one first register, each of the at least one first register storing information corresponding to a wireless device, and at least one second register; and,

an address portion, wherein the address portion includes control logic, whereupon loading of the second register with a data value, the control logic performs one of a read operation and a write operation with respect to a first register associated with the data value.

16. (New) The system recited in claim 15, wherein the control logic receives an input value corresponding to a desired field to be accessed in the register associated with the data value.

17. (New) The system recited in claim 15, wherein the wireless peripheral system further comprises a radio.

18. (New) The system recited in claim 16, wherein the control logic provides a signal indicating that a content of the desired field should be placed onto a data line.

19. (New) The system recited in claim 15, wherein the control logic receives an input value corresponding to a desired field to be written to the register associated with the data value.

20. (New) The system recited in claim 19, wherein the control logic provides a signal indicating that a signal on a data line should be written to the desired field in the register.